surface layer to a temperature between 1150°C and the melting temperature of said silicon substrate and melt said dopant layer and a top surface layer of said amorphous silicon layer to cause diffusion of said dopant into said top surface layer of said amorphous silicon layer and explosive recrystallization of said amorphous silicon layer to transform said amorphous layer into a polycrystalline silicon gate with said dopant distributed uniformly throughout said polycrystalline gate.

Remarks

Claims 1-6 and 9 were rejected by the Examiner under 35 USC §103(a) as being obvious over Xiang (6,159,782) in view of Talwar 6,274,488. The Examiner, in his discussion as to the applicability of the combination of Xiang and Talwar to claims 1-6 and 9, also addresses those references to claims 11 and 15-18. This is confusing since claims 15-18 are NOT included in this rejection, or any other of the specific rejections in the Examiner's Action. The actual rejection of claims 15-18 is merely included with the blanket summary of the rejections stated on the Office Action Summary page.

Claims 7, 12-14 and 19 were rejected by the Examiner under 35 USC §103(a) as being obvious over Xiang '782 in view of Talwar '488 and further in view of Microchip Fabrication by Van Zant. This specific rejection is also confusing given the Examiner's reference to claim18 in his explanation of the applicability of this rejection since claim 18 is NOT rejected in this specific rejection, or any of the four other specific grounds for rejection stated by the Examiner in his action. The only place where claim 18 is actually said to be rejected is on the Office Action Summary page.

Claims 8, 11, 20 and 21 were rejected by the Examiner under 35 USC §103(a) as being obvious over Xiang '782 in view of Talwar '488 and further in view of Ishida (5,966,605).

Claims 10 and 22 were rejected by the Examiner under 35 USC §103(a) as being obvious over Xiang '782 in view of Talwar '488 and further in view of Yu (6,159,782).

Claim 23 was rejected by the Examiner under 35 USC §103(a) as being obvious over Xiang '782 in view of Talwar '488 and further in view of Ishida and further in view of Zhang (6,077,758).

Claims 1 and 11 have been amended to put them in better condition for allowance.

Since the Examiner has included the combination of Xiang in view of Talwar in each of his specific rejections of the claims 1-14 and 19-23 (claims 15-18 have not been specifically rejected by the Examiner in the action to which this response is directed), and claims 1 and 11 are the only independent claims, the applicability of those two references will initially be discussed in relation to independent claims 1 and 11.

Each of claims 1 and 11 are for forming a doped polycrystalline silicon gate in a Metal Oxide Semiconductor (MOS) device formed on a top surface of a crystalline silicon substrate by forming an insulation layer on the top surface of the silicon substrate, and forming an amorphous silicon layer on top of and in contact with the insulation layer.

Then in amended claim 1 a dopant is introduced in a top surface layer of the amorphous silicon layer, with the amorphous silicon layer irradiated with a radiation beam to heat the top surface layer **to heat the top surface layer to a temperature between 1150°C and the melting temperature of the silicon substrate to initiate explosive recrystallization** of the amorphous silicon layer to transform the amorphous silicon layer into a polycrystalline silicon gate with the dopant distributed uniformly throughout the polycrystalline gate.

Similarly, in amended claim 11 a dopant layer is formed on top of and in contact with the amorphous silicon layer; with the amorphous silicon layer irradiated with a radiation beam to **heat the t p surface layer t a temperature between 1150°C and the melting temperature of the silicon substrate** and melt the dopant layer and a top surface layer of the amorphous silicon layer to cause diffusion of the dopant into the top surface layer of the amorphous silicon layer and **explosive recrystallization of the amorphous silicon layer** to transform the amorphous layer into a polycrystalline silicon gate with the dopant distributed uniformly throughout the polycrystalline gate.

Nowhere in Xiang is either of the terms "explosive crystallization" or "explosive recrystallization" used, and nowhere does Xiang even suggest that a temperature as high as 1150°C could be used to recrystallize the amorphous silicon layer to form a polycrystalline gate. Xiang talks only of "solid phase crystallization" of the amorphous gate layer at a temperature of about 600°C.

The phenomena of "explosive recrystallization" was well known for not less than fifteen years when Xiang filed his patent application on Aug. 5, 1999. Two papers published in well known and non-obscure journals on "explosive crystallization of silicon" fifteen and eleven years, respectively, prior to Xiang's filing date are (copies included herewith):

> Michael O. Thompson, G. J. Galvin, J. w. Mayer, P. S. Peercy, J. M. Poate, D.C. Jackobson, A. G. Cullis and N. G. Chew, "Melting temperature and explosive crystallization of amorphous silicon during pulsed laser irradiation", Physical Review Letters, Vol. 52, No. 26, 25 June 1984.
>
> P.S. Peercy and J. Y. Tsao, "Explosive crystallization in amorphous Si initiated by a long pulse width laser irradiation", Appl. Phys. Lett. 52(3), 18 January 1988.

Xiang discloses the performance of his anneal of the amorphous silicon gate material as follows:

> "The amorphous gate electrode material in the gate opening is then annealed at a **relatively low temperature, such as 600° Celsius**, using a **solid phase crystallization** process to convert the amorphous gate electrode material, such as amorphous silicon, into polycrystalline gate electrode material, such as polycrystalline silicon. Thus, **relatively low temperatures are used in the present invention to preserve the integrity of the gate dielectric having the high dielectric constant**." (emphasis added) (Abstract)

> "The amorphous gate electrode material in the gate opening is then annealed at a **relatively low temperature, such as 600° Celsius**, using a **solid phase crystallization** process to convert the amorphous gate electrode material, such as amorphous silicon, into polycrystalline gate electrode material, such as polycrystalline silicon." (emphasis added) (Col. 2, lines 61-67)

> "Such an anneal process converts the amorphous gate electrode material, such as amorphous silicon, to a polycrystalline gate electrode material, such as polycrystalline silicon. ... With low energy implantation of the N-type dopant for the NMOSFET 152 and the P-type dopant for the PMOSFET 102, a **solid phase crystallization** process using a **relatively low temperature of approximately 600° Celsius**, as known to one of ordinary skill in the art of integrated circuit fabrication, is used for the anneal process."

> "In this manner, fabrication processes after deposition of the gate dielectric having the high dielectric constant **use only relatively low**

temperatures such that the integrity f such a gate dielectric is preserved." (emphasis added) (Col. 8, lines 26-42)

Nowhere in Xiang can there be found mention of the any type of recrystallization other than "solid phase crystallization" even though "explosive crystallization was know at least 15 years prior to the filing of his patent application in 1999.

As evidenced by the Xiang patent he was living in Santa Clara, California and his co-inventor was living in Cupertino, California, and the patent is assigned to Advanced Micro Devices, Inc. of Sunnyvale, California. Since both Santa Clara and Cupertino are immediately adjacent to Sunnyvale, it is obvious that the inventors were in the employ of assignee, Advanced Micro Devices, Inc.

That being the case, since Advanced Micro Devices, Inc. is a major manufacturer of semiconductor devices and explosive crystallization had been known for at least 15 years prior to the filing date of their patent application, it is clear that Xiang. and his co-inventor, Lin, both must have been well aware of explosive crystallization of silicon, and thus, the careful clarification that the process used in their invention was "solid phase crystallization" at "a relatively low temperature" to "preserve the integrity of the gate dielectric having the high dielectric constant" was **purposefully done to distinguish there technique from explosive crystallization and to teach away from explosive crystallization which is performed at a higher temperature than solid phase crystallization**.

Had Xiang and Lin intended to introduce explosive crystallization as an alternative method for annealing an amorphous silicon gate they certainly would have done so and not gone to the trouble to clearly exclude the possibility of the use of explosive crystallization annealing from their patent.

Thus the method of the present invention using explosive recrystallization at the higher 1150+° Celsius temperature can not be said to be obvious from what has been disclosed by Xiang. Thus, independent claims 1 and 11, as amended, are not obvious from Xiang and distinguishable therefrom.

From the Examiner's rationale of his rejections and purpose for which he included Talwar with Xiang, it is clear that he does not find that Talwar discloses or suggests the methods disclosed in the present application, namely, the use of explosive crystallization to anneal an amorphous silicon gate in the production of a MOSFET. From the Examiner's explanation of his position in the rejection of claims 1 and 11 prior to the current amendment of those claims, Talwar is included with Xiang to show the use of a laser for the anneal process, but nothing else that is not shown or suggested by Xiang.

Therefore claims 1 and 11 as now amended are clearly distinguishable from Xiang and Talwar, taken alone or together. Thus, all of the claims, since they are dependent from either claim 1 or 11, are also distinguishable from Xiang and Talwar.

Additionally, none of the other references cited by the Examiner show or suggest what has been shown to be missing from either Xiang and Talwar, therefore claims 1 and 11, and all of the other claims pending in the present application, are patentable to the applicants since Xiang and Talwar are the primary references relied on by the Examiner in each of his specific rejections.

While it is possible to distinguish each of the claims from the various combinations of references used in each of the specific rejections cited by the Examiner, given that it has been shown that all of the claims are distinguishable from the two primary references cited in each of the specific rejections it is not necessary to provide the level of detail to show that all of the claims are patentable to the applicants over all

of the cited references.

All claims now being in condition for allowance, their allowance is respectfully requested.

Favorable action is respectfully requested.

Respectfully submitted,
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[thereby transforming] **to transf rm** said amorphous silicon layer into a polycrystalline silicon gate **[and distributing]** **with** said dopant **distributed** uniformly throughout said polycrystalline gate.

11. (Amended) A method of forming a doped polycrystalline silicon gate in a Metal Oxide Semiconductor (MOS) device formed on a top surface of a crystalline silicon substrate comprising:

a) forming an insulation layer on said top surface of the silicon substrate;

b) forming an amorphous silicon layer on top of and in contact with said insulation layer;

c) forming a dopant layer on top of and in contact with said amorphous silicon layer; and

d) irradiating said amorphous silicon layer with a radiation beam to heat **said top surface layer to a temperature between 1150°C and the melting temperature of said silicon substrate** and melt said dopant layer and a top surface layer of said amorphous silicon layer **[thereby causing]** **to cause** diffusion of said dopant into said top surface layer of said amorphous silicon layer and explosive recrystallization of said amorphous silicon layer **[thereby transforming]** **to transform** said amorphous layer into a polycrystalline silicon gate **[and distributing]** **with** said dopant **distributed** uniformly throughout said polycrystalline gate.